In re Patent Application of:
BREWER
Serial No. **09/674,444**
Filed: **OCTOBER 31, 2000**

REMARKS

Claims 1 to 3, 5 to 12 and 15 to 23 are currently pending. Claims 1, 2, 5 to 11, 15 to 17, 19 to 23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 4,975,634 (Shohet) in view of United States Patent No. 5,430,772 (Lee et al).

Applicant respectfully disagrees with the Examiner's assessment of the Shohet reference as related to the claims of the present invention. In particular, that the Shohet reference discloses "*detecting occasions when the number of sampling times in any bit of said digital signal is different from said predetermined number*". The method disclosed in the Shohet reference relies on the generation of **three** signals: the high frequency clock signal f_H, the reference clock signal f_R, and the jittered clock signal f_J. As disclosed in Column 3 lines 15 to 22 of Shohet:

The logic control 28 is responsive to a transition of the jittered clock signal f_J to enable a counter 26 to start counting the high frequency pulses f_H. Upon a transition of the reference clock signal f_R, the logic control stops the count. Therefore, the count represents the instantaneous phase difference between the jittered frequency f_J and the reference frequency f_R

Accordingly, Shohet only discloses counting the number of pulses in the high frequency pulse f_H that fall between the point when a pulse from the reference clock signal f_R starts (or stops) and the point when a pulse from the jittered clock signal f_J starts (or stops) to determine the instantaneous phase difference therebetween. These phase difference counts

are compared to each other to obtain a high and a low value, which are converted to jitter.

The present invention eliminates the need for both the f_H and f_R signals by counting the number of pulses from a reference clock signal that fall in **each bit** of the digital signal, and comparing that count to **a predetermined number** that would occur if there was no jitter. Then the number of times, when the number of sampling times in any bit of the digital signal is different from the predetermined number, is counted, and from this count the jitter is determined.

The present invention is much simpler than the device disclosed in the Shohet reference, i.e. does not require the hardware to generate both the high frequency clock signal f_H and the reference clock signal f_R, and enables an increase in analysis resolution, and the analysis of higher bit rates.

Furthermore, forming the "*offset reference clock signal… from said digital signal*", as defined by the claims of the present application, is also a novel and unobvious feature of the present invention not taught by the cited prior art. The device disclosed in the Shohet reference requires a separate source (Col 2, lines 54 to 57) for generating the high frequency clock signal, and requires hardware (reference clock generator 24) for converting the high frequency clock signal f_H into the reference clock signal f_R and the jitter free clock signal f_0. The present invention utilizes the digital signal, itself, to generate the reference clock signal, thereby eliminating the need and expense of a separate signal generator. Moreover, since the jittered digital signal is the input of the present invention, the jitter measurement device

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of the present invention can be easily added on to an existing test system after the Device Under Test (DUT), rather than making up the entire system before and after the DUT 10, as disclosed in the Shohet reference.

As such, it is respectfully submitted that all of the claims remaining in the application are in condition for allowance. Early and favorable consideration would be appreciated.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the COMMISSIONER FOR PATENTS, this 13 day of February 2006.